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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,457	09/10/2003	Murthi Nanja	Intel/17226	4880

75343 7590 06/11/2008

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EXAMINER	
DAO, THUY CHAN	
ART UNIT	PAPER NUMBER
2192	

MAIL DATE	DELIVERY MODE
06/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,457	NANJA ET AL.	
	Examiner	Art Unit	
	Thuy Dao	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-17 and 19-30* is/are pending in the application.

4a) Of the above claim(s) *2 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-17 and 19-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/14/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on April 14, 2008.

2. Claims 1, 3-17, and 19-30 have been examined.

Response to Amendments

3. In the instant amendments, claims 1, 3-4. 17-19, and 28 have been amended; claims 2 and 18 have been canceled.

Information Disclosure Statement

4. The Office acknowledges receipt of the Information Disclosure Statement filed on April 14, 2008. It has been placed in the application file and the information referred to therein has been considered by the examiner.

Specification

5. The specification is objected to because of minor informalities.

Per FIG. 2, these terms at least in pages 6-8 are considered to read as:

JIT memory location [[214]];

Thumb code generator [[216]] 214; and

ARM code generator [[218]] 216.

Appropriate correction for all pages is requested.

Furthermore, acronyms should be spelled out at the first appearance in the specification (e.g., page 2: "ARM", page 6: "MSIL", "JIT"; page 7: "POTS").

Appropriate correction is requested.

Claim Objections

6. Claim 10 is objected to because of minor informalities. Acronym "ARM" should be spelled out at the first appearance in claims.

Response to Arguments

7. Applicants' arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections – 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3-17, and 19-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,684,390 to Goff (art made of record, hereafter "Goff") in view of US Patent No. 7,013,456 to Van Dyke et al. (art made of record, hereafter "Van Dyke").

Claim 1:

Goff further discloses a *method of executing a non-native software instruction, the method comprising:*

receiving the non-native software instruction at a device (e.g., col.2: 4-27; FIG. 3, col.5: 44-57)*;*

generating a first native software instruction from a first instruction set based on the non-native software instruction (e.g., X86 instruction set, col.4: 55 – col.5: 18)*,*

the generation of the first native software instruction occurring at the device; executing the first native software instruction at the device (e.g., FIG. 2, col.4: 46 – col.5: 31).

Goff does not explicitly disclose other limitations. However, in an analogous art, Van Dyke further discloses:

executing the first native software instruction at the device (e.g., col.13: 17-32; X86-family processors; col.13: 45-53, native X86 instructions)*;*

counting a number of times the first native software instruction is executed (e.g., col.11: 19-40; col.13: 51-66)*;*

if the number of times the first native software instruction is executed exceeds a threshold (e.g., col.18: 57 – col.19: 4; col.45: 60-67)*,*

generating a second native software instruction from a second instruction set based on the non-native software instruction (e.g., col.13: 49-66 and col.14: 18-47, Tapestry/TAXi native instructions based on native X86 instructions; wherein said X86 native instructions based on said non-native instructions – please see Goff, col.4: 55 – col.5: 18 and FIG. 3, both X86 native instructions 220 and ARM native instructions 271-273 based on Java application 333)*,*

the generation of the second native software instruction occurring at the device (e.g., FIG. 1a, col.13: 17 – col.14: 47)*,*

wherein the second instruction set is different from the first instruction set; and executing the second native software instruction at the device (e.g., col.13: 49-66; col.14: 55 – col.15: 16).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Van Dyke's teaching into Goff's teaching. One would have been motivated to do so to provide a multi-processor Java subsystem as suggested by Goff (e.g., col.2: 5-36) and also provide two instruction set architectures, which can use a hot spot detector to translate and optimize binary execution as suggested by Van Dyke (e.g., col.4: 54 – col.5: 23; col.11: 19-40).

Claim 3:

The rejection of claim 1 is incorporated. Van Dyke further discloses *inserting instrumentation to count the number of times the first native software instruction is executed* (e.g., col.2: 8-23).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Van Dyke's teaching into Goff's teaching. One would have been motivated to do so as set forth above.

Claim 4:

The rejection of claim 1 is incorporated. Van Dyke further discloses *receiving the threshold via a mobile runtime configuration parameter* (e.g., col.18; 57 – col.19: 4).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Van Dyke's teaching into Goff's teaching. One would have been motivated to do so as set forth above.

Claim 5:

The rejection of claim 1 is incorporated. Goff discloses *receiving the non-native software instruction at the device comprises receiving an intermediate language instruction at the device* (e.g., col.2: 4-27; col.5: 44-57).

Claim 6:

The rejection of claim 1 is incorporated. Goff discloses *receiving the non-native software instruction at the device comprises receiving Java byte code at the device* (e.g., FIG. 2, col.5: 44-57).

Claim 7:

The rejection of claim 1 is incorporated. Van Dyke further discloses *receiving the non-native software instruction at the device comprises wirelessly receiving the non-native software instruction at a hand-held computing device* (e.g., col.2: 5-36; col.4: 55 – col.5: 18).

Claim 8:

The rejection of claim 1 is incorporated. Goff discloses *the first native software instruction comprises an X-bit wide instruction, the second native software instruction comprises a Y-bit wide instruction, and X is less than Y* (e.g., col.1: 43-49).

Claim 9:

The rejection of claim 1 is incorporated. Goff discloses *the first native software instruction comprises a 16-bit wide instruction, and the second native software instruction comprises a 32-bit wide instruction* (e.g., col.5: 5-19; col.7: 36-44).

Claim 10:

The rejection of claim 1 is incorporated. Goff discloses *the first native software instruction comprises a Thumb instruction, and the second native software instruction comprises an ARM instruction* (e.g., col.9: 47-54).

Claim 11:

The rejection of claim 1 is incorporated. Goff discloses *generating the first native software instruction comprises compiling the non-native software instruction at the device using a just-in-time compiler* (e.g., col.2: 5-36; col.5: 44-57).

Claim 12:

The rejection of claim 1 is incorporated. Van Dyke further discloses:

configuring a first code optimization option prior to generation of the first native software instruction, the first code optimization option causing smaller code to be generated (e.g., col.15, Table 1)*; and*

configuring a second code optimization option prior to generation of the second native software instruction, the second code optimization option causing faster code to be generated (e.g., col.14: 55 – col.15: 16).

Claim 13:

The rejection of claim 1 is incorporated. Van Dyke further discloses:

generating a first native software instruction comprises generating a first plurality of native software instructions (e.g., col.11: 19-40)*, and*

generating a second native software instruction comprises generating a second plurality of native software instructions (e.g., col.13: 51-66)*, the method further comprising:*

counting a first number of instructions contained within the first plurality of native software instructions; counting a second number of instructions contained within the second plurality of native software instructions (e.g., col.13: 49-66)*; and*

comparing the first number of instructions and the second number of instructions, wherein executing the first native software instruction is in response to one of (i) the second number of instructions equaling the first number of instructions (e.g., col.14: 18-47) *and*

(ii) the second number of instructions exceeding the first number of instructions (e.g., col.13: 49 – col.14: 47).

Claim 14:

The rejection of claim 13 is incorporated. Van Dyke further discloses:

comparing the first number of instructions and the second number of instructions (e.g., col.18: 57 – col.19: 4)*,*

wherein executing the second native software instruction is in response to the first number of instructions not exceeding the second number of instructions by more than a predetermined threshold (e.g., col.18: 40-67).

Claim 15:

The rejection of claim 1 is incorporated. Van Dyke further discloses:

measuring the first native software instruction resulting in a first number of bytes; measuring the second native software instruction resulting in a second number of bytes (e.g., col.13: 49-66)*; and*

comparing the first number of bytes and the second number of bytes, wherein executing the first native software instruction is in response to the first number

of bytes being less than the second number of bytes by at least a predetermined threshold (e.g., col.14: 55 – col.15: 16).

Claim 16:

The rejection of claim 1 is incorporated. Van Dyke further discloses:

measuring the first native software instruction resulting in a first number of bytes; measuring the second native software instruction resulting in a second number of bytes (e.g., col.11: 19-40)*; and*

comparing the first number of bytes and the second number of bytes, wherein executing the second native software instruction is in response to the first number of bytes not being less than the second number of bytes by at least a predetermined threshold (e.g., col.13: 51-66).

Claims 17 and 19-27:

Claims 17 and 19-27 recite the same limitations as those of claims 1 and 3-16, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the references teach all of the limitations of the above claims, they also teach all of the limitations of claims 17 and 19-27.

Claim 28:

Goff discloses *an apparatus structured to execute a mixed mode code, the apparatus comprising:*

a memory device; and a mixed mode processor operatively coupled to the memory device (e.g., col.2: 4-27; FIG. 3, col.5: 44-57),

the mixed mode processor being structured to execute a runtime environment, the runtime environment being stored in the memory device (e.g., FIG. 2, col.4: 46 – col.5: 31)*, the runtime environment comprising:*

a compiled binary; a first code generator to generate a first software instruction based on the compiled binary, the first software instruction being associated

with a first instruction set of the mixed mode processor (e.g., col.2: 5-36; col.5: 44-57; col.4: 46 – col.5: 31).

Goff does not explicitly disclose other limitations. However, in an analogous art, Van Dyke further discloses:

a compiled binary; a first code generator to generate a first software instruction based on the compiled binary (e.g., col.13: 17-32; col.13: 45-53),

the first software instruction being associated with a first instruction set of the mixed mode processor (e.g., col.11: 19-40; col.13: 51-66);

a counter to count a number of times the first software instruction is executed; a second code generator to generate a second software instruction (e.g., col.18: 57 – col.19: 4; col.45: 60-67)

based on the compiled binary if the number of times the first software instruction is executed exceeds a threshold (e.g., col.13: 49-66; col.14: 18-47),

the second software instruction being associated with a second instruction set of the mixed mode processor (e.g., FIG. 1a, col..13: 17 – col.14: 47),

wherein the first instruction set is different than the second instruction set; and an executing code including the first instruction and the second instruction (e.g., col.13: 49-66; col.14: 55 – col.15: 16).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Van Dyke's teaching into Goff's teaching. One would have been motivated to do so to provide a multi-processor Java subsystem as suggested by Goff (e.g., col.2: 5-36) and also provide two instruction set architectures, which can use a hot spot detector to translate and optimize binary execution as suggested by Van Dyke (e.g., col.4: 54 – col.5: 23; col.11: 19-40).

Claims 29-30:

Claims 29-30 recite the same limitations as those of claims 8-9, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the

references teach all of the limitations of the above claims, they also teach all of the limitations of claims 29-30.

Conclusion

10. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication should be directed to examiner Thuy Dao (Twee), whose telephone/fax numbers are (571) 272 8570 and (571) 273 8570, respectively. The examiner can normally be reached on every Tuesday, Thursday, and Friday from 6:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273 8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thuy Dao/
Examiner, Art Unit 2192

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192